AMENDMENTS

IN THE CLAIMS:

Claims 1-8. (Canceled).

9. (Previously presented) A transistor, comprising:

a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls;

a source region and a drain region in the substrate, wherein the source region and the drain region are formed using the gate structure as a mask, wherein the source region and the drain region each define a bottomwall junction at bottom portions thereof and a sidewall junction at sidewall portions thereof between the respective source and drain region and the substrate;

a channel defined in the substrate inwardly of the gate structure and between the source and drain regions; and

a bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through the bottomwall junction and the sidewall junction of the source region and the drain region.

10. (Original) The transistor of claim 9, wherein a concentration of dopants implanted to form the bottomwall/sidewall junction capacitance reduction region is about $1x10^{12}$ cm^{-2} to $1x10^{14}$ cm^{-2}.

11. (Original) The transistor of claim 9, wherein the transistor is an n-MOS type transistor and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 20-200 kV.

12. (Original) The transistor of claim 9, wherein the transistor is a p-MOS type transistor and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 30-100 kV.

13. (Original) The transistor of claim 9, wherein a non-encroachment distance is at least about 150 angstroms.

14. (Original) The transistor of claim 13, wherein at least a portion of the bottomwall/sidewall junction capacitance reduction region is implanted through the gate structure.

15. (Previously presented) A transistor, comprising:

a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls;

a source region and a drain region in the substrate, wherein the source region and the drain region are formed using the gate structure as a mask, wherein the source region and the drain region each define a bottomwall junction at bottom portions thereof and a sidewall junction at sidewall portions thereof between the respective source and drain region and the substrate;

a channel defined in the substrate inwardly of the gate structure and between the source and drain regions; and

a bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through the bottomwall junction, and

wherein a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaks substantially at the bottomwall junction.

16. (Original) The transistor of claim 9, wherein the bottomwall/sidewall junction capacitance reduction region is formed with the same mask configuration as is used during the formation of the source and drain regions.

17. (Previously presented) An integrated circuit comprising a plurality of metal oxide semiconductor field effect transistors (MOSFET), each MOSFET comprising:

a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls;

a source region and a drain region in the substrate, wherein the source region and the drain region are formed using the gate structure as a mask, wherein the source region and the drain region each define a bottomwall junction at bottom portions thereof and a sidewall junction at sidewall portions thereof between the respective source and drain region and the substrate;

a channel defined in the substrate inwardly of the gate structure and between the source and drain regions; and

a bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through the bottomwall junction and the sidewall junction of the source region and the drain region.

18. (Original) The integrated circuit of claim 17, wherein a concentration of dopants implanted to form the bottomwall/sidewall junction capacitance reduction region of each MOSFET is about $1x10^{12}$ cm^{-2} to $1x10^{14}$ cm^{-2}.

19. (Original) The integrated circuit of claim 17, wherein at least a portion of the bottomwall/sidewall junction capacitance reduction region of each MOSFET is implanted through the gate structure.

20. (Original) The integrated circuit of claim 17, wherein a dopant concentration of the bottomwall/sidewall junction capacitance reduction region of each MOSFET peaks substantially at the bottomwall junction.